# Dislocation microstructures on flat and stepped Si surfaces: Guidance for growing highquality GaAs on (100) Si substrates

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# Dislocation microstructures on flat and stepped Si surfaces: Guidance for growing high-quality GaAs on (100) Si substrates

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Type-I dislocations at the GaAs/Si interface are beneficial because they effectively relax the mismatched stress, but do not propagate into the GaAs film. Accordingly, the best way to grow a low defect density GaAs film on a Si substrate is to form as many as possible type-I dislocations or, equivalently, to suppress other kinds of defects. The high-resolution transmission electron microscopy study shows that most of the type-I dislocations are formed at the double step on a Si surface. It is further determined that the silicon surface steps are mainly due to the substrate tilting instead of the heating before growth. Based on our study, the (100) Si substrate with double steps along both [110] and [$1\bar{1}0$] axes provides the best condition for growing low defect density GaAs on Si substrates.

Considerable efforts have been made to achieve low defect GaAs epitaxy on Si substrates.[1,2] The state-of-the-art technology produces GaAs on Si films with a dislocation density from $10^6$ to $10^7$ cm$^{-2}$, which is still 1000 times higher than the dislocation density for GaAs films grown on GaAs substrates. Therefore, further improvement in film quality is necessary. To achieve this goal, knowledge of the defect microstructure is considered the most fundamental. This letter reports our study of the relationship between the dislocation structure and the silicon surface steps by means of high-resolution transmission electron microscopy (HRTEM). The results provide valuable information about the silicon surface structure most favorable for growing low defect GaAs films.

From the transmission electron microscopy (TEM) study, dislocations in the GaAs film are predominantly near the GaAs and Si interface. Even though most of the interface dislocations are confined at the interface to relax the misfit strain from lattice mismatch, some of the misfit dislocations propagate to the film surface as threading dislocations. Two major types of interface dislocations have been reported.[3,4] They are usually named as type-I and type-II dislocations. Type-I dislocations are ideal edge dislocations with Burgers vector 1/2[110] and the line vector [$1\bar{1}0$] or vice versa. Type-I dislocations are "beneficial" because they effectively relax the mismatch stress, but do not degrade the film. However, type-II dislocations, having their Burgers vectors 1/2[101], 1/2[$10\bar{1}$], 1/2[011], or 1/2[$01\bar{1}$], and line vectors [$1\bar{1}0$] or [110], lie in the {111} planes and very probably propagate to the film surface as complete dislocations or by dissociating into partial dislocations. If the dissociation of type-II dislocations happens, one partial is left at the interface, but the other partial propagates to the GaAs film surface. The areas between these two partials are stacking faults. Furthermore, type-II dislocations have only 70% of the total Burgers vectors in the misfit plane so that they are not so effective to release the strain. Therefore, the occurrence of type-II dislocations should be minimized because it is harmful to the film quality. The critical issue on GaAs/Si heteroepitaxy technology is to look for an efficient way to release the misfit strain by predominately type-I dislocations or to suppress type-II dislocations as much as possible.

The previous HRTEM study of the defect microstructure suggests that type-I dislocations tend to be formed at the flat silicon surface, but type-II dislocations more frequently occur at the stepped silicon surface.[4] However, the experimental results reported by Otsuka *et al.* showed that the ratio of type-I to type-II dislocation is obviously higher along the artificially tilted step-rich axis than along the flat axis.[4] To explain this controversy, we specifically investigate the relationship between type-I dislocation and silicon surface structure by HRTEM.

The (100) silicon substrate with 4° misorientation

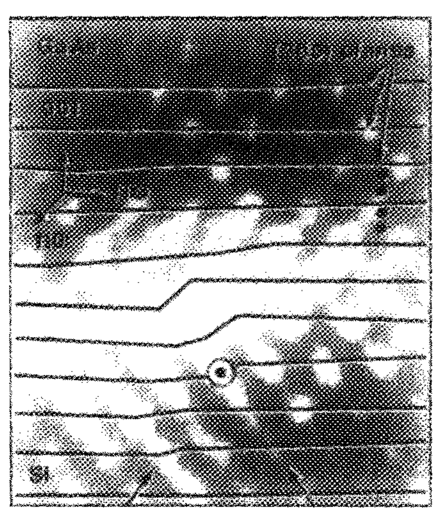


FIG. 1. HRTEM lattice image of a type-I dislocation. The arrows indicate two extra {111} planes in silicon lattice. A series of (200) planes obtained by connecting the discrete points along the [$1\bar{1}0$] direction is also shown. The deformation of (200) planes asymmetric to the dislocation core reveals that this dislocation is at a stepped Si surface.

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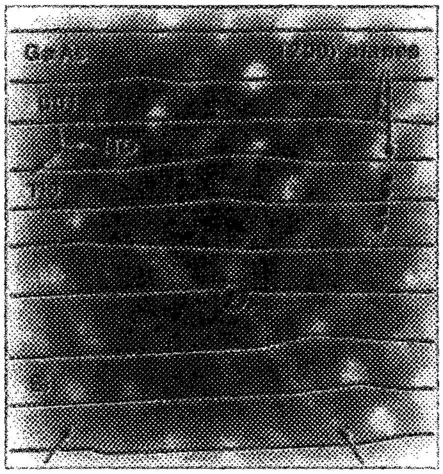

FIG. 2. HRTEM lattice image of a type-I dislocation. A series of (200) planes is obtained in a similar way as in Fig. 1. The slight deformation of (200) planes symmetric to the dislocation core shows that this dislocation is at a flat Si surface.

towards ⟨110⟩ axis is cleaned and heated to 800 or 900 °C for 20 min to remove the thin oxide. The first 200 Å GaAs layer is deposited at about 350 °C. The sample is then heated to 600 °C to grow the subsequent GaAs layer up to 3 $\mu$m. From the cross-section HRTEM pictures, both types of dislocations are found, and the stress from lattice mismatch is almost completely relaxed by the interface misfit dislocations. Figures 1 and 2 show the magnified lattice images of two different dislocations of type I. As marked in Figs. 1 and 2, the cores of both dislocations are formed at the intersections of two inclined extra Si {111} planes which results in the Burgers vectors being parallel to the interface. In order to determine if the dislocation is formed at a stepped or flat Si surface, the lattice deformation around dislocation core is carefully investigated next.

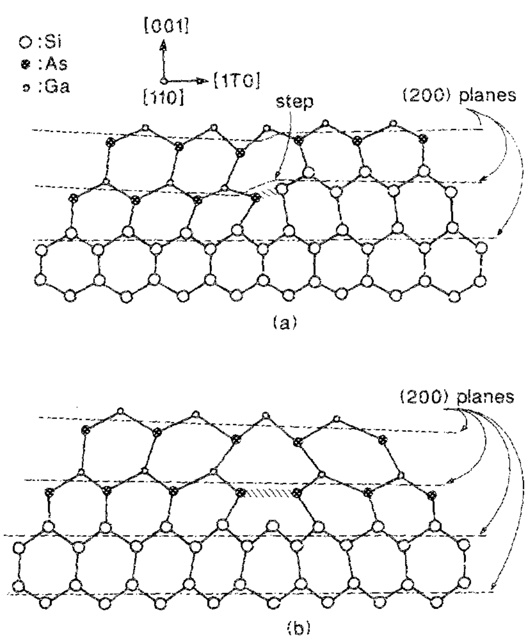


FIG. 3. Dislocation microstructure constructed from Figs. 1 and 2. Note that the dash lines in (a) and (b), representing the (200) planes, show characteristics similar to those in Figs. 1 and 2, respectively.

TABLE I. Number of type-I dislocations found on various Si surfaces.

| Si surface | Number of type I dislocations |
|---|---|
| Stepped | 8 |
| Flat | 1 |

The model structure for a type-I dislocation on a stepped and a flat silicon surface is illustrated in Figs. 3(a) and 3(b). We construct the lattice structure, keeping in mind that the bonding energy is ordered as $E_{\text{Si-Si}} > E_{\text{Si-As}} > E_{\text{As-Ga}}$ and the weakest bond tends to be most seriously deformed under tension.[5,6] The bonding between Ga and Si is not taken into account in Fig. 3 since recent experiments revealed that the Si surface is predominantly bonded with As atoms. The dash lines in Figs. 3(a) and 3(b) represent a series of (200) planes. The (200) planes are deformed in Fig. 3(a) asymmetric to the core if the dislocation is at a double-stepped surface. However, the (200) planes are only slightly deformed in Fig. 3(b) if the dislocation is at a flat surface. Any surface step will not obviously alter the local deformation of the (200) planes near core unless it is very close to the core. Judged from the extent and the symmetry of the (200) lattice plane deformation, the silicon surface structure for type-I dislocations can be determined. The dislocation in Fig. 1 is identified at a double-stepped Si surface with the lattice structure shown in Fig. 3(a) since its (200) planes are deformed asymmetrical to the core. On the other hand, the dislocation in Fig. 2 is considered to occur at a flat surface with the structure shown in Fig. 3(b) because its very slight (200) plane deformation is symmetric to the core.

As shown in Table I, only one out of nine dislocations which are investigated is at the flat Si surface, and all others are formed at the stepped surface, although the number of atoms at steps is less than one-tenth of that at flat parts of the surface. This result leads to the conclusion that type-I dislocations are favorably formed at the double-stepped Si surface. Furthermore, the silicon surface steps in the eight pictures are all towards the same direction, with their right-hand side higher than their left-hand sides. This phenomenon helps us to ascertain the origin of the steps on a silicon surface. If the 800–900 °C thermal treatment before growth is the main reason for step generation, all of the steps should not be aligned in one direction. On the contrary, the steps will be directionally aligned if they are mainly produced by intentional sample tilting. Our experimental data out of these eight steps indicate that the silicon surface steps are predominantly generated by intentional sample tilting rather than thermal treatment even if the tilting angle is only 4°.

In summary, we conclude that the type-I dislocation is preferentially formed at the stepped silicon surface, and the steps are predominantly generated by intentional sample tilting. This conclusion explains why the ratio of type-I to type-II dislocations along the tilted axis is higher than that along the flat axis. To grow low dislocation density GaAs film on Si substrates, we propose to use the (100) silicon substrate with double steps in both [110] and [1$\bar{1}$0] directions. The appropriate tilting direction is important not only in the elimination of antiphase domains, but also very critical in the reduction of the ultimate dislocation density for the GaAs film grown on Si substrates.

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